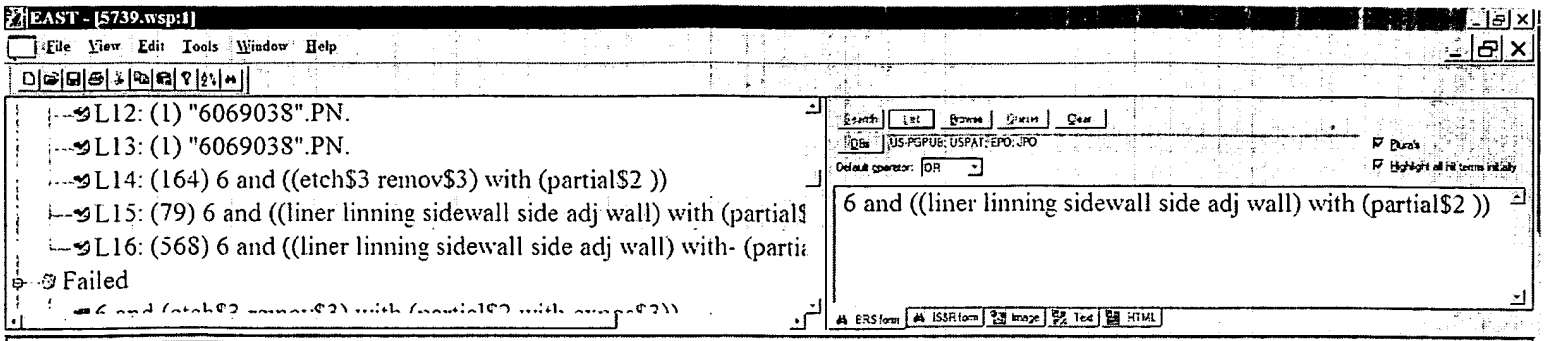
Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L3	2472	(stack$3 near3 gate) with (sidewall side near3 wall spacer linning liner)	US-PGPUB; USPAT; EPO; JPO	OR	ON	2005/06/01 13:21
L4	1876	3 and ((etch$3 remov$3) with (sidewall side near3 wall spacer linning liner))	US-PGPUB; USPAT; EPO; JPO	OR	ON	2005/06/01 13:22
L5	715	4 and (bitline bit adj line)	US-PGPUB; USPAT; EPO; JPO	OR	ON	2005/06/01 13:23
L6	605	5 and ((dielectric insulat$3) with (opening trench hole contact via))	US-PGPUB; USPAT; EPO; JPO	OR	ON	2005/06/01 13:24
L7	56	6 and ((etch$3 remov$3) with (partial$2 with expos$3))	US-PGPUB; USPAT; EPO; JPO	OR	ON	2005/06/01 13:40
L8	1	"6365497".PN.	USPAT; USOCR	OR	ON	2005/06/01 13:32
L9	1	"6168984".PN.	USPAT; USOCR	OR	ON	2005/06/01 13:35
L10	1	"6127260".PN.	USPAT; USOCR	OR	ON	2005/06/01 13:35
L11	1	"6117725".PN.	USPAT; USOCR	OR	ON	2005/06/01 13:36
L12	1	"6069038".PN.	USPAT; USOCR	OR	ON	2005/06/01 13:36
L13	1	"6069038".PN.	USPAT; USOCR	OR	ON	2005/06/01 13:37
L14	164	6 and ((etch$3 remov$3) with (partial$2))	US-PGPUB; USPAT; EPO; JPO	OR	ON	2005/06/01 13:40
L15	79	6 and ((liner linning sidewall side adj wall) with (partial$2))	US-PGPUB; USPAT; EPO; JPO	OR	ON	2005/06/01 13:40

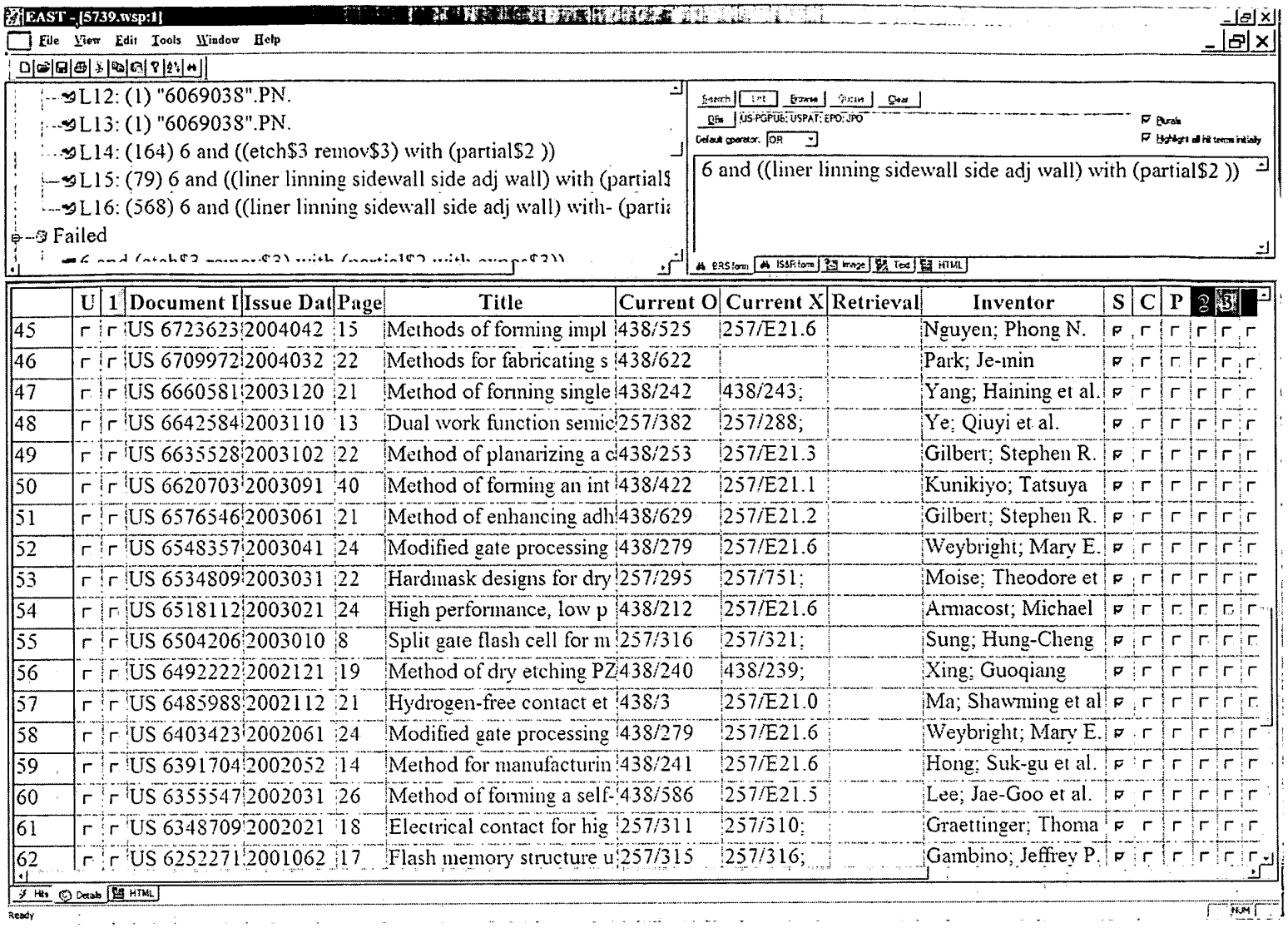
S16	2166	(stack$3 near3 gate) with (sidewall side near3 wall spacer)	US-PGPUB; USPAT; EPO; JPO	OR	ON	2005/01/03 07:31
S17	2188	(stack$3 near3 gate) with (sidewall side near3 wall spacer linning liner)	US-PGPUB; USPAT; EPO; JPO	OR	ON	2005/06/01 13:21
S18	1606	S17 and (etch$3 with (sidewall side near3 wall spacer linning liner))	US-PGPUB; USPAT; EPO; JPO	OR	ON	2005/06/01 13:22
S19	1364	S17 and silicide	US-PGPUB; USPAT; EPO; JPO	OR	ON	2004/12/27 12:52
S20	511	S19 and (bitline bit adj line)	US-PGPUB; USPAT; EPO; JPO	OR	ON	2005/06/01 13:23
S21	441	S20 and ((dielectric insulat$3) with (opening trench hole contact via))	US-PGPUB; USPAT; EPO; JPO	OR	ON	2005/06/01 13:24
S22	319	S21 and (etch$3 with (partial$2 wiht expos$3))	US-PGPUB; USPAT; EPO; JPO	OR	ON	2005/06/01 13:25
S23	319	S22 and gate	US-PGPUB; USPAT; EPO; JPO	OR	ON	2004/12/27 12:57
S24	317	S23 and substrate	US-PGPUB; USPAT; EPO; JPO	OR	ON	2004/12/27 13:08
S25	195	S24 and (gate with cap$4)	US-PGPUB; USPAT; EPO; JPO	OR	ON	2004/12/27 13:09
S26	1	"6066541".PN.	USPAT; USOCR	OR	ON	2004/12/27 16:20
S27	1	"6043529".PN.	USPAT; USOCR	OR	ON	2004/12/27 16:20

S28	1	"5989952".PN.	USPAT; USOCR	OR	ON	2004/12/27 16:20
S29	1	"5972747".PN.	USPAT; USOCR	OR	ON	2004/12/27 16:20
S30	1	"5929526".PN.	USPAT; USOCR	OR	ON	2004/12/27 16:20
S31	1	"6136651".PN.	USPAT; USOCR	OR	ON	2004/12/27 16:31
S32	1	"5998262".PN.	USPAT; USOCR	OR	ON	2004/12/27 16:31
S33	9	10/038845	US-PGPUB; USPAT; EPO; JPO	OR	ON	2004/12/28 16:33
S34	0	"10899024"	US-PGPUB; USPAT; EPO; JPO	OR	ON	2004/12/28 16:33
S35	0	"10/899024"	US-PGPUB; USPAT; EPO; JPO	OR	ON	2004/12/28 16:35
S36	1	"6835966"	US-PGPUB; USPAT; EPO; JPO	OR	ON	2004/12/28 16:51
S37	0	10/899024	US-PGPUB; USPAT; EPO; JPO	OR	ON	2004/12/28 16:36
S38	7	"6580098"	US-PGPUB; USPAT; EPO; JPO	OR	ON	2004/12/28 16:52
S39	45	"6121121"	US-PGPUB; USPAT; EPO; JPO	OR	ON	2004/12/28 16:52
S40	1	"6365921".PN.	USPAT; USOCR	OR	ON	2004/12/28 17:28
S41	1	"6355497".PN.	USPAT; USOCR	OR	ON	2004/12/28 17:28

S42	1	"6146457".PN.	USPAT; USOCR	OR	ON	2004/12/28 17:28
S43	1	"6121121".PN.	USPAT; USOCR	OR	ON	2004/12/28 17:28
S44	1	"6380108".PN.	USPAT; USOCR	OR	ON	2004/12/28 18:26
S45	1	10/654449	US-PGPUB; USPAT; EPO; JPO	OR	ON	2005/01/03 07:31



	U	1	Document I	Issue Dat	Page	Title	Current O	Current X	Retrieval	Inventor	S	C	P	2	3
63	☐	☐	US 6239011	2001052	12	Method of self-aligned co	438/595	257/E21.2		Chen; Bi-Ling et al.	☑	☐	☐	☐	☐
64	☐	☐	US 6232185	2001051	25	Method of making a float	438/266	257/E21.2		Wang; Ching D.	☑	☐	☐	☐	☐
65	☐	☐	US 6211091	2001040	6	Self-aligned eetching pro	438/706	438/710;		Lien; Wan-Yih et al	☑	☐	☐	☐	☐
66	☐	☐	US 6207977	2001032	63	Vertical MISFET devices	257/192	257/19;		Augusto; Carlos Jor	☑	☐	☐	☐	☐
67	☐	☐	US 6204112	2001032	9	Process for forming a hig	438/243	257/E21.6		Chakravarti; Ashim	☑	☐	☐	☐	☐
68	☐	☐	US 6198144	2001030	18	Passivation of sidewalls o	257/412	257/623;		Pan; Pai-Hung et al.	☑	☐	☐	☐	☐
69	☐	☐	US 6090673	2000071	19	Device contact structure	438/301	257/E21.5		Allen; Archibald J.	☑	☐	☐	☐	☐
70	☐	☐	US 5963800	1999100	60	CMOS integration proces	438/212	257/334;		Augusto; Carlos Jor	☑	☐	☐	☐	☐
71	☐	☐	US 5920088	1999070	61	Vertical MISFET devices	257/192	257/194;		Augusto; Carlos Jor	☑	☐	☐	☐	☐
72	☐	☐	US 5914504	1999062	60	DRAM applications usin	257/192	257/195;		Augusto; Carlos Jor	☑	☐	☐	☐	☐
73	☐	☐	US 5907780	1999052	12	Incorporating silicon ato	438/299	257/E21.1		Gilmer; Mark C. et	☑	☐	☐	☐	☐
74	☐	☐	US 5828602	1998102	56	Memory system having m	365/185.2	257/E21.6		Wong; Chun Chiu	☑	☐	☐	☐	☐
75	☐	☐	US 5821143	1998101	16	Fabrication methods for n	438/267	257/E21.6		Kim; Jae-youn et al.	☑	☐	☐	☐	☐
76	☐	☐	US 5739567	1998041	56	Highly compact memory	257/316	257/320;		Wong; Chun Chiu	☑	☐	☐	☐	☐
77	☐	☐	US 5717635	1998021	14	High density EEPROM f	365/185.0	257/314;		Akatsu; Hiroyuki	☑	☐	☐	☐	☐
78	☐	☐	US 5616510	1997040	56	Method for making multi	438/259	257/E21.6		Wong; Chun C. D.	☑	☐	☐	☐	☐
79	☐	☐	US 5386132	1995013	58	Multimedia storage syste	257/316	257/320;		Wong; Chun C. D.	☑	☐	☐	☐	☐



	U	1	Document I	Issue Dat	Page	Title	Current O	Current X	Retrieval	Inventor	S	C	P	2	3
45	☐	☐	US 6723623	2004042	15	Methods of forming impl	438/525	257/E21.6		Nguyen; Phong N.	☑	☐	☐	☐	☐
46	☐	☐	US 6709972	2004032	22	Methods for fabricating s	438/622			Park; Je-min	☑	☐	☐	☐	☐
47	☐	☐	US 6660581	2003120	21	Method of forming single	438/242	438/243;		Yang; Haining et al.	☑	☐	☐	☐	☐
48	☐	☐	US 6642584	2003110	13	Dual work function semic	257/382	257/288;		Ye; Qiuyi et al.	☑	☐	☐	☐	☐
49	☐	☐	US 6635528	2003102	22	Method of planarizing a c	438/253	257/E21.3		Gilbert; Stephen R.	☑	☐	☐	☐	☐
50	☐	☐	US 6620703	2003091	40	Method of forming an int	438/422	257/E21.1		Kunikiyo; Tatsuya	☑	☐	☐	☐	☐
51	☐	☐	US 6576546	2003061	21	Method of enhancing adh	438/629	257/E21.2		Gilbert; Stephen R.	☑	☐	☐	☐	☐
52	☐	☐	US 6548357	2003041	24	Modified gate processing	438/279	257/E21.6		Weybright; Mary E.	☑	☐	☐	☐	☐
53	☐	☐	US 6534809	2003031	22	Hardmask designs for dry	257/295	257/751;		Moise; Theodore et	☑	☐	☐	☐	☐
54	☐	☐	US 6518112	2003021	24	High performance, low p	438/212	257/E21.6		Armacost; Michael	☑	☐	☐	☐	☐
55	☐	☐	US 6504206	2003010	8	Split gate flash cell for m	257/316	257/321;		Sung; Hung-Cheng	☑	☐	☐	☐	☐
56	☐	☐	US 6492222	2002121	19	Method of dry etching PZ	438/240	438/239;		Xing; Guoqiang	☑	☐	☐	☐	☐
57	☐	☐	US 6485988	2002112	21	Hydrogen-free contact et	438/3	257/E21.0		Ma; Shawming et al	☑	☐	☐	☐	☐
58	☐	☐	US 6403423	2002061	24	Modified gate processing	438/279	257/E21.6		Weybright; Mary E.	☑	☐	☐	☐	☐
59	☐	☐	US 6391704	2002052	14	Method for manufacturin	438/241	257/E21.6		Hong; Suk-gu et al.	☑	☐	☐	☐	☐
60	☐	☐	US 6355547	2002031	26	Method of forming a self-	438/586	257/E21.5		Lee; Jae-Goo et al.	☑	☐	☐	☐	☐
61	☐	☐	US 6348709	2002021	18	Electrical contact for hig	257/311	257/310;		Graettinger; Thoma	☑	☐	☐	☐	☐
62	☐	☐	US 6252271	2001062	17	Flash memory structure u	257/315	257/316;		Gambino; Jeffrey P.	☑	☐	☐	☐	☐

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L13: (1) "6069038".PN.
L14: (164) 6 and ((etch$3 remov$3) with (partial$2))
L15: (79) 6 and ((liner linning sidewall side adj wall) with (partial$
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	U	1	Document I	Issue Dat	Page	Title	Current O	Current X	Retrieval	Inventor	S	C	P	2	3
26			US 2002010	2002080	14	Dual work function semic	257/10	257/261;		Ye, Qiuyi et al.					
27			US 2002007	2002061	22	Method of enhancing adh	438/629	257/E21.2		Gilbert, Stephen R.					
28			US 2002006	2002053	17	Passivation of sidewalls o	257/344	257/E21.2		Pan, Pai-Hung et al.					
29			US 2002005	2002051	14	METHOD FOR MANUF	438/241	257/E21.6		Hong, Suk-Gu et al.					
30			US 2002000	2002012	25	High performance, low p	257/330	257/E21.6		Armacost, Michael					
31			US 2002000	2002011	21	Hydrogen-free contact et	438/3	257/E21.0		Ma, Shawming et al					
32			US 2001004	2001112	22	Method of planarizing a c	438/653	257/E21.3		Gilbert, Stephen R.					
33			US 2001003	2001102	22	Hardmask designs for dry	438/396	257/E21.0		Moise, Theodore et					
34			US 2001000	2001060	25	HIGH PERFORMANCE,	257/327	257/E21.6		ARMACOST, MIC					
35			US 6897145	2005052	24	Method for fabricating se	438/637	438/250;		Park; Je-Min					
36			US 6878991	2005041	26	Vertical device 4F2 EEP	257/328	257/316;		Forbes; Leonard					
37			US 6872640	2005032	20	SOI CMOS device with r	438/514	257/347;		Mouli; Chandra V.					
38			US 6844591	2005011	24	Method of forming DRA	257/330	257/332		Tran; Luan C.					
39			US 6815290	2004110	17	Stacked gate flash memor	438/257	438/259;		Lin; Chi-Hui et al.					
40			US 6806187	2004101	17	Electrical contact for hig	438/675	438/240;		Graettinger; Thoma					
41			US 6768164	2004072	17	Stacked gate flash memor	257/321	257/401;		Lin; Chi-Hui et al.					
42			US 6767789	2004072	30	Method for interconnecti	438/254	257/306;		Bronner; Gary B. et					
43			US 6744089	2004060	23	Self-aligned lateral-transi	257/301	257/296;		Wu; Ching-Yuan					

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L14: (164) 6 and ((etch$3 remov$3) with (partial$2))
L15: (79) 6 and ((liner linning sidewall side adj wall) with (partial$
L16: (568) 6 and ((liner linning sidewall side adj wall) with- (parti
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6 and ((liner linning sidewall side adj wall) with (partial$2))

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	U	1	Document I	Issue Dat	Page	Title	Current O	Current X	Retrieval	Inventor	S	C	P	2	3
8	☐	☐	US 2005000	2005010	32	Recess type transistor an	257/330	257/619;		Kim, Ji-Young	☑	☐	☐	☐	☐
9	☐	☐	US 2004026	2004123	15	Interconnect line selectiv	257/296	257/308;		Drynan, John M.	☑	☐	☐	☐	☐
10	☐	☐	US 2004019	2004100	15	Semiconductor structure	438/294			Lee, Yueh-Chuan et	☑	☐	☐	☐	☐
11	☐	☐	US 2004012	2004062	22	Stacked gate flash memor	438/257	257/E29.3		Lin, Chi-Hui	☑	☐	☐	☐	☐
12	☐	☐	US 2004010	2004061	14	Dual work function semic	257/382	257/E21.5		Ye, Qiuyi et al.	☑	☐	☐	☐	☐
13	☐	☐	US 2004010	2004061	17	STACKED GATE FLAS	257/316	257/315;		Lin, Chi-Hui et al.	☑	☐	☐	☐	☐
14	☐	☐	US 2004010	2004061	17	Interconnect line selectiv	257/300			Drynan, John M.	☑	☐	☐	☐	☐
15	☐	☐	US 2004007	2004042	18	Stacked gate flash memor	257/324	257/E21.4		Lin, Chi-Hui et al.	☑	☐	☐	☐	☐
16	☐	☐	US 2004005	2004032	34	Bitline of semiconductor	257/44			Jeong, Mun-Mo et a	☑	☐	☐	☐	☐
17	☐	☐	US 2004004	2004031	26	SELF-ALIGNED LATER	257/301	257/E29.3		Wu, Ching-Yuan	☑	☐	☐	☐	☐
18	☐	☐	US 2004002	2004021	25	Method for fabricating se	438/142			Park, Je-Min	☑	☐	☐	☐	☐
19	☐	☐	US 2003023	2003122	23	Methods for fabricating s	438/253	438/255;		Park, Je-min	☑	☐	☐	☐	☐
20	☐	☐	US 2003007	2003042	17	Interconnect line selectiv	438/618	438/622;		Drynan, John M.	☑	☐	☐	☐	☐
21	☐	☐	US 2003006	2003041	31	Process for manufacturin	257/324	257/405;		Caprara, Paolo et al	☑	☐	☐	☐	☐
22	☐	☐	US 2002018	2002121	17	Interconnect line selectiv	438/253			Drynan, John M.	☑	☐	☐	☐	☐
23	☐	☐	US 2002013	2002092	41	Semiconductor integrated	257/510	257/E21.1		Kunikiyo, Tatsuya	☑	☐	☐	☐	☐
24	☐	☐	US 2002013	2002091	8	Novel split gate flash cell	257/316	257/E21.2		Sung, Hung-Cheng	☑	☐	☐	☐	☐
25	☐	☐	US 2002011	2002081	26	Modified gate processing	438/689	257/E21.6		Weybright, Mary E.	☑	☐	☐	☐	☐

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